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TRANSMITTAL FORM

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First Named Inventor	Kenneth W. Marr
Art Unit	2815
Examiner Name	N. Drew Richards
Attorney Docket Number	2269-3543US (97-0952.00/US)

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) ____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Brief (23 pages); Claims Appendix (13 pages); Check no. 9608 in the amount of $500.00
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below)*:

Decision in Application Serial No. 09/277,893, dated February 10, 2005

Decision in Application Serial No. 09/702,583, dated December 31, 2003

Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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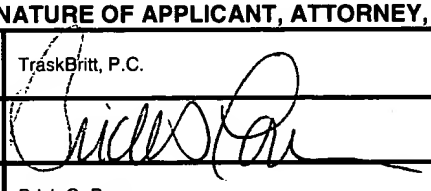
Signature			
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Kenneth W. Marr

Serial No.: 09/277,893

Filed: March 29, 1999

For: SEMICONDUCTOR FUSES, SEMICONDUCTOR DEVICES CONTAINING THE SAME, AND METHODS OF MAKING AND USING THE SAME

Confirmation No.: 4223

Examiner: N. Drew Richards

Group Art Unit: 2815

Attorney Docket No.: 2269-3543US

NOTICE OF EXPRESS MAILING

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APPEAL BRIEF

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Attn: Board of Patent Appeals and Interferences

Sir:

This APPEAL BRIEF is being submitted in the format required by 37 C.F.R. § 41.37(c)(1), with the fee required by 37 C.F.R. § 41.20(b)(2).

1. REAL PARTY IN INTEREST

U.S. Application Serial No. 09/277,893 (hereinafter "the '893 Application"), the patent application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc. (hereinafter "Assignee"). The assignment has been recorded with the United States Patent & Trademark Office (hereinafter "the Office") at Reel No. 9878, Frame No. 0785. Accordingly, Micron Technology, Inc. is the real party in interest to the referenced appeal.

2. RELATED APPEALS AND INTERFERENCES

The Board of Patent Appeals and Interferences (hereinafter "the Board") issued a Decision on an appeal of final rejections presented in the '893 Application on February 14, 2005.

A Decision on an appeal of the final rejections that were presented in U.S. Application Serial No. 09/702,583, which was filed on October 31, 2000, as a divisional of the '893 Application was issued by the Board on December 31, 2003.

There are no pending appeals, interferences, or other actions that are believed to directly affect or be affected by the Board's decision in the '893 Application.

3. STATUS OF CLAIMS

The '893 Application was filed with one-hundred and one (101) claims. Claims 1-16, 34-49, and 73 have been canceled from the '893 Application without prejudice or disclaimer. Claims 102-105 were subsequently introduced.

No claims have been allowed.

The final rejections of claims 17-33, 50-72, and 74-101 are being appealed.

4. STATUS OF AMENDMENTS

Initially, the '893 Application included one-hundred and one (101) claims.

A Restriction Requirement was made on October 3, 2000. Pursuant to an election without traverse to prosecute claims 17-33 and 50-101 in a communication dated October 19, 2000, claims 1-16 and 34-49 were withdrawn from consideration. Claims 1-16 and 34-49 were subsequently canceled without prejudice or disclaimer in an Amendment dated February 26, 2001.

A first Office Action on the merits was mailed on December 21, 2000. Each of claims 17-33 and 50-101 was rejected in the first Office Action. In a responsive Amendment, which was dated February 26, 2001, several claim amendments were presented, along with reasoning as to the allowability of the amended claims over the art that had been relied upon in the first Office Action. In particular, claims 17, 50, and 71 were amended, as were several dependent claims. In addition, claim 73 was canceled without prejudice or disclaimer.

Next, a first Final Office Action was mailed on April 12, 2001. Again, each of the claims that remained pending and under consideration in the '893 Application was rejected, including claims 17-33, 50-72, and 74-101. In response, an Amendment Under 37 C.F.R. § 1.116 was filed on May 29, 2001, in which further explanations as to the allowability of claims 17-33, 50-72, and 74-101 were provided and another amendment to claim 71 was proposed.

In an Advisory Action dated June 7, 2001, several of the claim rejections were maintained. A Request for Continued Examination was subsequently filed on June 12, 2001.

A third, non-final Office Action was mailed on June 12, 2001. In the third Office Action, each of claims 17-33, 50-72, and 74-101 was again rejected. On October 17, 2001, another response was filed. No additional claim amendments were made in that response.

The Office replied with a second Final Office Action on November 27, 2001. The response thereto, an Amendment Under 37 C.F.R. § 1.116 filed on January 11, 2002, included proposed amendments to each of independent claims 17, 50, and 71. In an Advisory Action, which was mailed on January 29, 2002, the Office refused to enter the proposed claim amendments. In order to cause the proposed claim amendments to be entered, a second Request for Continued Examination was filed on February 7, 2002.

On April 16, 2002, another non-final Office Action, the fifth Office Action in the '893 Application, was mailed. Again, each of claims 17-33, 50-72, and 74-101 was rejected. Again, the Office remained unconvinced by the reasoning provided in the response thereto, which was dated July 16, 2002.

As a result, the Office mailed a sixth, Final Office Action on August 21, 2002. The previous reasoning as to the patentability of claims 17-33, 50-72, and 74-101 was reiterated and enhanced in a response dated October 17, 2002.

Nonetheless, in an Advisory Action that was mailed on October 31, 2002, the rejections of claims 17-33, 50-72, and 74-101 were maintained.

The continued rejection of the claims resulted in the filing of an appeal in the '893 Application. After an Appeal Brief, Examiner's Answer, and Reply Brief had been entered into the file for the '893 Application, the Board refused to hear the appeal, as an English translation of a non-English reference had not been provided to Appellants before the Notice of

Appeal was filed. After an English translation of that reference was provided, the Board considered the appeal and issued a Decision on February 14, 2005.

Thereafter, on April 11, 2005, in consideration of the Board's Decision and the guidance provided therein, Appellants filed a Request for Continued Examination (RCE) and an accompanying amendment, in which several revisions to the claims were presented. That amendment was followed by a Supplemental Amendment dated April 26, 2006, in which additional revisions were made to the claims, and new claims 102-105 were added.

On June 26, 2005, a non-final action was mailed. All of the previously presented rejections were maintained.

A Response to that action was submitted on September 29, 2005. The Response clearly set forth the reasons that the pending claims are allowable over the art upon which the Examiner's rejections are based.

Nonetheless, on December 8, 2005, a final action was issued.

In a response dated February 8, 2006, Appellants made one last attempt to convince the Examiner of the patentability of the pending claims.

An Advisory Action was mailed on March 15, 2006, to indicate that the Examiner was unwilling to allow any of the claims.

Accordingly, a Notice of Appeal was filed on March 24, 2006. This Appeal Brief follows the Notice of Appeal and is being filed within two months of the mailing date of the Notice of Appeal.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The '893 Application describes and claims methods for fabricating fuses. A fuses that is fabricated in accordance with the inventive methods includes terminals with a lower layer of conductive material, such as a metal or conductively doped polysilicon, and an upper layer that comprises a metal silicide or polycide. Page 4, lines 14-16; page 7, lines 9-12; FIGs. 7 and 8. A central, or fusible, region of the fuse, which is located between two terminals thereof, comprises the metal silicide or polycide but not the other conductive material. Page 4, lines 14-16; page 7, lines 12-15; FIGs. 7 and 8.

In fabricating the fuse, a layer of the conductive material may be deposited adjacent to an insulative structure, such as a field oxide region of a semiconductor device structure. Page 5, lines 8-10; page 9, lines 9-15; FIG. 3. The layer of conductive material is patterned to define at least two spaced apart terminal sites. Page 4, line 27, to page 5, line 1; page 5, lines 10-12; page 9, line 16, to page 10, line 14; FIG. 4.

A layer of the metal silicide or polycide is formed over the layer of conductive material. Page 5, lines 15-19; page 10, line 15, to page 11, line 6; FIG. 5. The layer of metal silicide or polycide is patterned to define the upper layers of the fuse terminals and the central region of the fuse. Page 5, lines 19-25; page 11, line 7, to page 12, line 3; FIG. 6. The material volume of each terminal may exceed the material volume of the central region of the fuse. Page 5, lines 25-27. The central region of the fuse may also be narrower than the terminals thereof. Page 11, lines 17-19.

6. GROUNDS OF REJECTION TO BE REVIEWED

(A) The rejection of claims 17, 19-24, 26-33, 102, and 103 under 35 U.S.C. § 103(a) for reciting subject matter that is allegedly unpatentable over teachings from U.S. Patent 5,185,291 to Fischer et al. (hereinafter "Fischer"), in view of the teachings of U.S. Patent 5,712,206 to Chen (hereinafter "Chen");

(B) The 35 U.S.C. § 103(a) rejection of claim 18 for being directed to subject matter that is purportedly unpatentable over teachings from Fischer, in view of the teachings of Chen and, further, in view of the subject matter taught in Japanese Patent No. 59-154,038 to Mitani (hereinafter "Mitani");

(C) The 35 U.S.C. § 103(a) rejection of claim 25 for being drawn to subject matter that is assertedly unpatentable over the subject matter taught in Fischer and Chen, in view of teachings from U.S. Patent No. 5,231,056 to Sandhu (hereinafter "Sandhu");

(D) The rejection of claims 50, 51, 55-60, and 62-68 under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over a combination of teachings of Fischer, Mitani, and Chen;

(E) The 35 U.S.C. § 103(a) rejection of claims 52-54, 69, and 70 for reciting subject matter that is allegedly unpatentable over combined teachings from Fischer, Mitani, Chen, and U.S. Patent 5,242,859 to Degelormo et al. (hereinafter "Degelormo");

(F) The rejection of claim 61 under 35 U.S.C. § 103(a) for being directed to subject matter that is assertedly unpatentable over the teachings of Fischer, Mitani, Chen, and Sandhu;

(G) The rejection of claims 71, 74-86, 88-96, 101, 104, and 105 under 35 U.S.C. § 103(a) for being drawn to subject matter that is purportedly unpatentable over the subject matter taught in Mitani, Fischer, and Chen;

(H) The 35 U.S.C. § 103(a) of claim 72 for reciting subject matter which is assertedly unpatentable over a combination of teachings from Mitani, Fischer, Chen, and Degelormo;

(I) The rejection of claim 87 under 35 U.S.C. §103(a) for being directed to subject matter that is purportedly unpatentable over the teachings of Mitani, Fischer, Chen, and Sandhu; and

(J) The rejection of claims 97-100 under 35 U.S.C. § 103(a) for reciting subject matter that is allegedly unpatentable over a combination of teachings from Mitani, Fischer, Chen, and U.S. Patent 6,069,055 to Ukeda et al. (hereinafter "Ukeda").

7. ARGUMENT

Each of claims 17-33, 50-72, and 74-105 has been rejected under 35 U.S.C. § 103(a).

A. APPLICABLE LAW

The standard for establishing, maintaining, and upholding a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim

> limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant=s disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

B. REFERENCES RELIED UPON

Fischer

Fischer teaches a fuse for use in a semiconductor device structure, as well as a process for fabricating the fuse. The fuse of Fischer, which is disposed over an insulative structure (*i.e.,* dielectric 10) (*see, e.g.,* FIGs. 1-4; col. 2, lines 29-36), includes a first conductive layer 11 and a second conductive layer 12. The first conductive layer 11 of the finished fuse may be formed from aluminum or tungsten (col. 2, lines 43-45) and includes two end regions (FIG. 3). The second conductive layer 12 of the fuse may be formed from the same material as the first layer 11 or from polysilicon. Col. 2, lines 59-63. In a finished fuse, such as that illustrated in FIG. 3 of Fischer, end portions of the second conductive layer 12 overlie the two end regions of the first conductive layer 11, while the central portion 111 of the second conductive layer 12 is located in substantially the same plane as the first conductive layer 11 and between portions of the first conductive layer 11. *See also,* col. 2, lines 56-58.

Fischer teaches that the fuse is fabricated by forming a first layer of conductive material 11 over an insulative structure 10 (FIG. 1; col. 2, lines 45-48), patterning a "window" 111 in the first layer of conductive material to expose a portion of the underlying insulative structure (FIG. 1; col. 2, lines 36-38; col. 3, lines 34-55), forming a second layer 12 of conductive material over the first layer 11 and within the window 111 (FIG. 2; col. 2,

lines 49-55), and patterning the "combined" first and second layers to form the fuse (FIG. 3; col. 2, lines 56-58).

The teachings of Fischer are limited to methods for fabricating a multi-layer fuse, the upper layer of which is configured to be "blown" to program the fuse. None of the layers of that fuse comprises metal silicide. Nor does Fischer provide one of ordinary skill in the art with any motivation to use metal silicide to form one of the layers of the fuse described therein.

Chen

Chen also teaches a fuse and a method for fabricating the fuse. The fuse of Chen may be formed from aluminum, titanium tungsten, a silicide or polycide, or polysilicon (col. 5, lines 59-63), but only includes a single material layer.

A portion of the fuse described in Chen is exposed by way of a so-called fuse "window." *See, e.g.,* col. 4, lines 50-54. This "window" facilitates programming of the fuse with a laser. *See* col. 7, lines 38-40. In order to prevent contamination of the fuse prior to programming thereof, as well as to prevent contamination of the underlying semiconductor device features following programming of the fuse, Chen teaches a method for forming a moisture barrier both above and beneath the window of the fuse.

Mitani

Mitani teaches a fuse with lower layer that is formed from polycrystalline silicon and an upper layer with spaced apart regions that are formed from a metal silicide, as well as methods for fabricating such a fuse. Mitani, Abstract. In the fabrication method, the polycrystalline

silicon is first deposited on a field oxide. *Id.* Next, a layer of metal silicide is formed over the polycrystalline silicon, and the layers are etched in combination. *Id.* Finally, the intermediate part of the metal silicide is etched, leaving only polycrystalline silicon as the central region of the finished fuse, the portion of the fuse that is to be ruptured. *Id.*

Sandhu

Sandhu teaches a process for depositing a tungsten silicide film on a substrate using chemical vapor deposition (CVD).

Degelormo

Degelormo merely teaches a CVD method for forming layers of conductively doped polysilicon. Degelormo includes no teaching or suggestion that the CVD process thereof may be used to fabricate any part of a fuse or structures associated directly with a fuse.

Ukeda

Ukeda teaches a dry etch process for anisotropically removing exposed regions of a polysilicon layer through a metal silicide layer. Ukeda does not teach or suggest that the process disclosed therein may be used to fabricate a fuse.

C. ANALYSIS

i. Fischer in View of Chen

Claims 17, 19-24, 26-33, 102, and 103 have been rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over the subject matter taught in Fischer, in view of teachings from Chen.

It is respectfully submitted that a *prima facie* case of obviousness has not been established with respect to the subject matter recited in any of claims 17, 19-24, 26-33, 102, and 103. Without the benefit of hindsight that the claims and disclosure of the '893 Application have provided to the Examiner, one of ordinary skill in the art wouldn't have been motivated to combine the teachings of Fischer and Chen in the manner that has been asserted.

The teachings of Fischer are limited to methods for fabricating fuses with multiple conductive layers, none of which includes a silicide. Neither Fischer nor Chen provides one of ordinary skill in the art with any reason to substitute a silicide for one of the conductive layers of the fuse of Fischer. In fact, the teachings and suggestions of Fischer are limited to use of aluminum, tungsten, or polysilicon for the programmable portion 12 of the fuse. Col. 2, lines 43-45, 59-63.

The teachings of Chen, in contrast, are limited to fuses that comprise a single layer of sicilide. Neither Chen nor Fischer includes any teaching or suggestion that would have provided one of ordinary skill in the art with any reason to add an additional layer of conductive material at either terminal end of the single layer silicide fuse taught in Chen. Such modification would have merely unnecessarily increased the complexity of the fuse fabrication process of Chen.

From the teachings of Fischer and Chen, it is apparent that without the benefit of hindsight that has been afforded to the Examiner, one of ordinary skill in the art would have had no motivation to combine teachings from Fischer and Chen in the manner that has been asserted. Further, no teachings that were generally available to those of ordinary skill in the art at the appropriate time have been supplied to show otherwise. As such, it is clear that the 35 U.S.C. § 103(a) rejection of claims 17, 19-24, 26-33, 102, and 103 is based entirely upon an improper hindsight reconstruction of the subject matter recited in these claims.

Moreover, by touting the usefulness of aluminum, tungsten, or polysilicon for use in forming the programmable portion of the fuse described therein, Fischer teaches away from the asserted motivation to substitute a silicide for one of these materials in the programmable portion of a fuse.

Therefore, a *prima facie* case of obviousness of claims 17, 19-24, and 26-33 has not been established pursuant to the requirements of 35 U.S.C. § 103(a). Accordingly, claims 17, 19-24, 26-33, 102, and 103 are drawn to subject matter that is allowable over the teachings of Fischer and Chen.

ii. Fischer, Chen, and Mitani

Claim 18 is rejected under 35 U.S.C. § 103(a) for being drawn to subject matter that is purportedly unpatentable over teachings from Fischer, in view of the teachings of Chen and, further, in view of the subject matter taught in Mitani.

Claim 18 is allowable, among other reasons, as depending from claim 17, which is allowable.

Moreover, Mitani does not remedy the deficiencies that have been noted previously herein with respect to the asserted combination of Fischer and Chen. Specifically, one of ordinary skill in the art wouldn't have been motivated to combine the teachings of Mitani with those of Fischer or Chen in the manner that has been asserted by the Examiner.

The teachings of Fischer are limited to methods for fabricating a multi-layer fuse, the upper layer of which is configured to be "blown" to program the fuse. None of the layers of that fuse comprises metal silicide. Nor does Fischer provide one of ordinary skill in the art with any motivation to use metal silicide to form one of the layers of the fuse described therein.

Chen teaches a method for forming a single-layer fuse from a variety of materials, including metal silicide, but does not provide one of ordinary skill in the art with any motivation to also use another conductive material and, thus, multiple layers at the ends, or terminals, of the fuse.

While Mitani includes the combined use of a metal silicide layer with a polysilicon layer, Mitani teaches that the upper metal silicide layer, not the lower polysilicon layer, is patterned to form terminal regions. Thus, it is the lower polysilicon layer of the fuse of Mitani, not the upper metal silicide layer of that fuse, that forms the region of the fuse which is to be ruptured.

One of ordinary skill in the art wouldn't have been motivated to combine teachings from Fischer, Chen, and Mitani in the asserted manner because none of these references would have provided one of ordinary skill in the art with any clear guidance as to the function of metal silicide as the fusible element of a multi-layered fuse.

For these reasons, one of ordinary skill in the art wouldn't have been motivated, either by the teachings of Fischer, Chen, and Mitani, or by the knowledge that was available to one or

ordinary skill in the art prior to the filing date of the '893 Application, to combine the teachings of Fischer, Chen, and Mitani in the manner that has been asserted.

Any such motivation could only have been improperly gleaned from the hindsight which the description of the '893 Application provides.

Furthermore, one of ordinary skill in the art wouldn't have had any reason to expect that combining the methods described in Fischer, Chen, and Mitani would result in the method that is recited in claim 18. This is primarily due to directive provided in M.P.E.P. § 2141.02 that, in combining reference teachings, the teachings of the references must be considered in their entireties. Due to the extreme divergence between the methods of Fischer, Chen, and Mitani, there is no way all of the teachings of these references could be considered in developing a fuse fabrication method such as that recited in claim 18. The most likely result of such a combination would resemble the method taught in Mitani, without removal of material of the metal silicide layer from the region of the fuse which is configured to rupture during patterning of the metal silicide layer.

As a *prima facie* case of obviousness has not been set forth, claim 18 recites subject matter which is allowable over teachings from Fischer, Chen, and Mitani.

iii. Fischer, Chen, and Sandhu

Claim 25 stands rejected under 35 U.S.C. § 103(a) for being directed to subject matter that is allegedly unpatentable over the teachings of Fischer, in view of the subject matter taught in Chen and, further, in view of teachings from U.S. Patent 5,231,056 to Sandhu (hereinafter "Sandhu").

Sandhu teaches a process for depositing a tungsten silicide film on a substrate using chemical vapor deposition.

Claim 25 is allowable, among other reasons, as depending from claim 17, which is allowable. Claim 25 is further allowable since Sandhu, which merely teaches a process for depositing a tungsten silicide film by chemical vapor deposition, does not provide any teaching or suggestion that remedies the aforementioned deficiencies in the asserted combination of Fischer and Chen.

iv. Fischer, Mitani, and Chen

Claims 50, 51, 55-60, and 62-68 have been rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over the subject matter taught in Fischer, in view of teachings from Mitani and, further, in view of teachings from Chen.

The reasons that one of ordinary skill in the art wouldn't have been motivated to combine the teachings of these references in the asserted manner and the reasons that one of ordinary skill in the art would have no reason to expect the asserted combination to be successful have been set forth above.

For these same reasons, the asserted combination of Fischer, Mitani, and Chen cannot support a *prima facie* case of obviousness, pursuant to 35 U.S.C. ' 103(a), against independent claim 50. Therefore, under 35 U.S.C. ' 103(a), independent claim 50, as well as each of claims 51, 55-60, and 62-68, which depend either directly or indirectly from claim 50, is allowable over the subject matter taught in Fischer, Mitani, and Chen.

v. Fischer, Mitani and Chen in View of Degelormo

Claims 52-54, 69, and 70 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter that is allegedly unpatentable over the subject matter taught in Fischer, in view of teachings from Mitani, Chen, and U.S. Patent 5,242,859 to Degelormo et al. (hereinafter "Degelormo").

The teachings of Fischer, Mitani, and Chen have been summarized previously herein.

Degelormo merely teaches a chemical vapor deposition (CVD) method for forming layers of conductively doped polysilicon. Degelormo includes no teaching or suggestion that the CVD process thereof may be used to fabricate any part of a fuse or structures associated directly with a fuse.

As Degelormo merely teaches a CVD method for forming layers of conductively doped polysilicon without teaching or suggesting that the CVD process thereof may be used to fabricate any part of a fuse or structures associated directly with a fuse, Degelormo includes no teaching or suggestion that would remedy the deficiencies of Fischer, Mitani, and Chen with respect to their inabilities to have provided one of ordinary skill in the art with the requisite motivation to make the asserted combination of reference teachings.

Nor do the teachings of Degelormo provide one of ordinary skill in the art with any additional reason to believe that the teachings of Fischer, Mitani, Chen, and Degelormo could be successfully combined to provide a method for fabricating a fuse.

Furthermore, claims 52-54, 69, and 70 are each allowable, among other reasons, as depending from claim 50, which is allowable.

Therefore, under 35 U.S.C. § 103(a), claims 52-54, 69, and 70 are directed to subject matter which is allowable over the teachings of Fischer, Mitani, Chen, and Degelormo. As such, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 52-54, 69, and 70 be withdrawn.

vi. Fischer, Mitani, Chen, and Sandhu

Claim 61 stands rejected under 35 U.S.C. § 103(a) for being drawn to subject matter which is assertedly unpatentable over that taught in Fischer, Mitani, Chen, and Sandhu.

As explained previously herein, Sandhu does not provide any teaching or suggestion that remedies the deficiencies that have been identified herein with respect to the asserted combination of Fischer and Chen. For the same reasons, as well as those discussed previously herein with respect to the asserted combination of Fischer, Mitani, and Chen, Sandhu would not remedy the deficiencies that have been noted regarding the asserted combination of Fischer, Mitani, and Chen. Therefore, a *prima facie* case of obviousness cannot be established against claim 61 based merely upon the asserted combination of teachings from Fischer, Mitani, Chen, and Sandhu.

Claim 61 is also allowable, among other reasons, for depending from claims 50 and 60, which are allowable.

vii. Mitani, Fischer, and Chen

Claims 71, 74-86, 88-96, 101, 104, and 105 are rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over the teachings of Mitani, in view of teachings from Fischer and Chen.

Independent claim 71 recites a method of fabricating a gate and a fuse that includes patterning regions of a layer of polysilicon to form laterally discrete, spaced apart regions of polysilicon around and between which an underlying field oxide region is exposed.

For the same reasons provided previously herein, one of ordinary skill in the art wouldn't have been motivated to combine the teachings of Mitani, Fischer, and Chen in the asserted manner. Moreover, for reasons presented previously herein, one of ordinary skill in the art would have had no reason to believe that combining the teachings of these references would result in the method recited in claims 71, 74-86, 88-96, and 101 of the '893 Application.

Therefore, a *prima facie* case of obviousness cannot be established based on the teachings of Mitani, Chen, and Fischer. Therefore, under 35 U.S.C. § 103(a), the subject matter recited in claims 71, 74-86, 88-96, 101, 103, and 104 is allowable over the subject matter taught in Mitani, Chen, and Fischer.

viii. Mitani, Fischer and Chen in View of Degelormo

Claim 72 stands rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Mitani, Fischer, Chen, and Degelormo.

Claim 72 is allowable, among other reasons, as depending from claim 71, which is allowable.

ix. Mitani, Fischer and Chen in View of Sandhu

Claim 87 is rejected under 35 U.S.C. § 103(a) for being directed to subject matter that is purportedly unpatentable over the subject matter taught in Mitani, Fischer, Chen, and Sandhu.

Claim 87 is allowable, among other reasons, as depending from claim 71, which is allowable.

x. Mitani, Fischer and Chen in View of Ukeda

Claim 97-100 have been rejected under 35 U.S.C. § 103(a) for being drawn to subject matter which is allegedly unpatentable over teachings from Mitani, Fischer, Chen, and U.S. Patent 6,069,055 to Ukeda et al. (hereinafter "Ukeda").

Ukeda teaches a dry etch process for anisotropically removing exposed regions of a polysilicon layer through a metal silicide layer. Ukeda does not teach or suggest that the process disclosed therein may be used to fabricate a fuse.

It is clear that Ukeda does not remedy the deficiencies of Mitani, Chen, and Fischer, and the knowledge that was generally available in the art prior to the filing date of the '893 Application with respect to providing some motivation to one of ordinary skill in the art to combine the teachings of these references. It is also clear that Ukeda does not include any teaching that would give one of ordinary skill in the art a reasonable basis for expecting the combination of Mitani, Chen, Fischer, and Ukeda to provide a successful method for fabricating a fuse.

Claims 97-100 are each allowable, among other reasons, as depending from claim 71, which should be allowed.

Reversal of the 35 U.S.C. § 103(a) rejections of claims 17-33, 50-72, 74-105 is respectfully requested.

(8) CLAIMS APPENDIX

A listing of claims 1-77 is attached as the CLAIMS APPENDIX to this APPEAL BRIEF.

(9) EVIDENCE APPENDIX

There is no EVIDENCE APPENDIX to this APPEAL BRIEF.

(10) RELATED PROCEEDINGS APPENDIX

Copies of the above-mentioned Descisions of the Board are included in the RELATED PROCEEDINGS APPENDIX to this APPEAL BRIEF.

(11) CONCLUSION

It is respectfully submitted that:

(A) Claims 17, 19-24, 26-33, 102, and 103 are allowable under 35 U.S.C. § 103(a) over Fischer and Chen;

(B) Claim 18 recites subject matter which is allowable under 35 U.S.C. § 103(a) over Fischer, Chen, and Mitani;

(C) Claim 25 is allowable under 35 U.S.C. § 103(a) as reciting subject matter which is patentable over Fischer, Chen, and Sandhu;

(D) Claims 50, 51, 55-60, and 62-68 are allowable under 35 U.S.C. § 103(a) as reciting subject matter which is allowable over Fischer, Mitani, and Chen;

(E) Claims 52-54, 69, and 70 recite subject matter which is patentable under 35 U.S.C. § 103(a) over Fischer, Mitani, Chen, and Degelormo;

(F) Claim 61 is allowable for reciting subject matter which, under 35 U.S.C. § 103(a), is patentable over Fischer, Mitani, Chen, and Sandhu;

(G) Claims 71, 74-86, 88-96, 101, 104, and 105 are allowable under 35 U.S.C. § 103(a) as being patentable over Mitani, Fischer, and Chen;

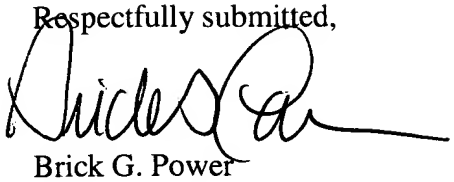
(H) Claim 72 is patentable, under 35 U.S.C. § 103(a), for reciting subject matter which is allowable over the combination of Mitani, Fischer, Chen, and Degelormo;

(I) Claim 87 recites subject matter which is patentable under 35 U.S.C. §103(a) over Mitani, Fischer, Chen, and Sandhu; and

(J) Claims 97-100 recite subject matter which is patentable under 35 U.S.C. § 103(a) as being nonobvious over Mitani, Fischer, Chen, and Ukeda.

Accordingly, reversal of the rejections of claims 17-33, 50-72, and 74-105 under 35 U.S.C. § 103(a) is respectfully solicited.

Respectfully submitted,



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CLAIMS APPENDIX

1-16 (Canceled)

17. A method of fabricating a fuse upon a semiconductor device, comprising:

disposing a layer of conductive material over an insulative structure of the semiconductor device;

patterning said layer of conductive material to define at least two spaced apart terminal sites;

removing conductive material of said layer in areas around said spaced apart terminal sites;

disposing a layer of metal silicide over the semiconductor device, including adjacent to said insulative structure exposed between said at least two terminal sites; and

patterning said layer of metal silicide so as to define at least two terminal regions of the fuse, each of which is in contact with a corresponding one of said at least two terminal sites of conductive material, and a central region disposed between said at least two terminal regions and in contact with said insulative structure.

18. The method of claim 17, wherein said disposing said layer of conductive material comprises disposing polysilicon onto said insulative structure.

19. The method of claim 17, wherein said patterning said layer of conductive material comprises disposing a mask over the semiconductor device and removing selected regions of said layer of conductive material through said mask.

20. The method of claim 19, wherein said disposing said mask comprises:

disposing photoresist onto the semiconductor device;

exposing selected regions of said photoresist; and

developing said selected regions.

21. The method of claim 19, wherein said removing comprises etching said selected regions of said layer of conductive material through said mask.

22. The method of claim 21, wherein said etching comprises isotropically etching said selected regions.

23. The method of claim 21, wherein said etching comprises wet etching said selected regions of said layer of conductive material.

24. The method of claim 17, wherein said disposing said layer of conductive material comprises chemical vapor depositing said layer of conductive material.

25. The method of claim 17, wherein said depositing said layer of metal silicide comprises chemical vapor depositing said layer of metal silicide.

26. The method of claim 17, wherein said depositing said layer of metal silicide comprises depositing tungsten silicide.

27. The method of claim 17, wherein said patterning said layer of metal silicide comprises disposing a mask over the semiconductor device and removing selected regions of said layer of metal silicide through said mask.

28. The method of claim 27, wherein said disposing said mask comprises:

disposing photoresist over the semiconductor device;

exposing selected regions of said photoresist; and

developing said selected regions.

29. The method of claim 27, wherein said removing comprises etching said selected regions of said layer of metal silicide.

30. The method of claim 29, wherein said etching comprises anisotropically etching said selected regions of said layer of metal silicide.

31. The method of claim 29, wherein said etching comprises dry etching said selected regions of said layer of metal silicide.

32. The method of claim 17, further comprising disposing a contact in communication with at least one of said at least two terminal regions.

33. The method of claim 32, further comprising disposing another contact in communication with another of said at least two terminal regions.

34-49 (Canceled)

50. A method of fabricating a fuse, comprising:

fabricating spaced apart terminal sites comprising polysilicon on an insulative structure of a semiconductor device, said insulative structure being exposed between each of said spaced apart terminal sites; and

fabricating a fuse comprising a metal silicide, including a central region disposed adjacent the insulative structure and between said spaced apart terminal sites and at least two terminal regions disposed on opposite ends of the central region and adjacent said spaced apart terminal sites.

51. The method of claim 50, wherein said fabricating spaced apart terminal sites comprises:

disposing polysilicon onto said insulative structure; and

patterning said polysilicon.

52. The method of claim 51, wherein said disposing polysilicon comprises chemical vapor depositing polysilicon.

53. The method of claim 51, further comprising doping said polysilicon.

54. The method of claim 53, wherein said doping occurs substantially simultaneously with said disposing.

55. The method of claim 51, wherein said patterning comprises disposing a mask adjacent said polysilicon and removing selected regions of said polysilicon through said mask.

56. The method of claim 55, wherein said disposing said mask comprises disposing photoresist adjacent said polysilicon, exposing selected regions of said photoresist, and developing said selected regions.

57. The method of claim 55, wherein said removing selected regions of said polysilicon comprises etching said selected regions.

58. The method of claim 57, wherein said etching comprises isotropically etching said selected regions.

59. The method of claim 57, wherein said etching comprises wet etching said selected regions.

60. The method of claim 50, wherein said fabricating said fuse comprises disposing metal silicide adjacent said spaced apart terminal sites and said insulative structure exposed therebetween.

61. The method of claim 60, wherein said disposing metal silicide comprises chemical vapor depositing metal silicide.

62. The method of claim 60, wherein said fabricating said fuse further comprises patterning said metal silicide.

63. The method of claim 62, wherein said patterning comprises disposing a mask adjacent said metal silicide and removing selected regions of said metal silicide through said mask.

64. The method of claim 63, wherein said disposing said mask comprises disposing photoresist adjacent said metal silicide, exposing selected regions of said photoresist, and developing said selected regions.

65. The method of claim 63, wherein said removing selected regions of said metal silicide comprises etching said selected regions of said metal silicide.

66. The method of claim 65, wherein said etching comprises anisotropically etching said selected regions.

67. The method of claim 65, wherein said etching comprises dry etching said selected regions.

68. The method of claim 62, wherein said patterning comprises defining said at least two terminal regions of the fuse adjacent said spaced apart terminal sites and said central region of the fuse adjacent said insulative structure.

69. The method of claim 50, further comprising doping said spaced apart terminal sites of polysilicon.

70. The method of claim 69, wherein said doping occurs substantially simultaneously with disposing polysilicon on said insulative structure.

71. A method of substantially simultaneously fabricating a gate and a fuse on a semiconductor substrate, comprising:

disposing a layer of insulative material over at least an exposed region of the semiconductor substrate;

disposing a layer of polysilicon over the semiconductor substrate, including over said layer of insulative material and over isolation regions disposed on the semiconductor substrate;

patterning at least regions of said layer of polysilicon disposed over at least one isolation region of said isolation regions to define at least two spaced apart terminal sites from said polysilicon over said at least one isolation region with at least a portion of said at least one isolation region being exposed between said spaced apart terminal sites;

removing polysilicon of said layer from areas of said layer located around said at least two spaced apart terminal sites;

disposing a layer of metal silicide on said layer of polysilicon and into contact with said portion of said at least one isolation region;

patterning at least said layer of metal silicide to define the fuse and the gate therefrom.

72. The method of claim 71, wherein said disposing said layer of polysilicon comprises chemical vapor depositing said layer of polysilicon.

73 (Canceled)

74. The method of claim 71, wherein said defining the fuse comprises defining a central region disposed adjacent and substantially between said at least two spaced apart terminal sites and defining at least two terminal regions, each terminal region continuous with an end of said central region and disposed adjacent one of said at least two spaced apart terminal sites.

75. The method of claim 71, wherein said defining said at least two spaced apart terminal sites comprises disposing a mask over said layer of polysilicon and removing selected regions of said layer of polysilicon through said mask.

76. The method of claim 75, wherein said disposing said mask comprises disposing photoresist over said layer of polysilicon, exposing selected regions of said photoresist, and developing said selected regions.

77. The method of claim 75, wherein said removing comprises etching said layer of polysilicon.

78. The method of claim 77, wherein said etching comprises wet etching said layer of polysilicon.

79. The method of claim 77, wherein said etching comprises isotropically etching said layer of polysilicon.

80. The method of claim 71, further comprising patterning gate regions of said layer of polysilicon.

81. The method of claim 80, wherein said patterning said gate regions occurs substantially simultaneously with said patterning said at least regions of said layer of polysilicon.

82. The method of claim 80, wherein said patterning said gate regions comprises disposing a mask over said layer of polysilicon and removing selected regions of said layer of polysilicon through said mask.

83. The method of claim 82, wherein said disposing said mask comprises disposing photoresist over said layer of polysilicon, exposing selected regions of said photoresist, and developing said selected regions.

84. The method of claim 82, wherein said removing comprises etching said selected regions.

85. The method of claim 84, wherein said etching comprises dry etching said selected regions.

86. The method of claim 84, wherein said etching comprises anisotropically etching said selected regions.

87. The method of claim 71, wherein said disposing said layer of metal silicide comprises chemical vapor depositing said layer of metal silicide.

88. The method of claim 71, wherein said defining the fuse and the gate from at least said layer of metal silicide comprises disposing a mask over said layer of metal silicide and removing selected regions of said layer of metal silicide through said mask.

89. The method of claim 88, wherein said disposing said mask comprises disposing photoresist over said layer of metal silicide, exposing selected regions of said photoresist, and developing said selected regions.

90. The method of claim 88, wherein said removing said selected regions comprises etching said selected regions.

91. The method of claim 90, wherein said etching comprises dry etching said selected regions.

92. The method of claim 90, wherein said etching comprises anisotropically etching said selected regions.

93. The method of claim 71, further comprising removing exposed regions of polysilicon through said layer of metal silicide.

94. The method of claim 93, wherein said removing comprises etching said exposed regions.

95. The method of claim 94, wherein said etching comprises dry etching said exposed regions.

96. The method of claim 94, wherein said etching comprises anisotropically etching said exposed regions.

97. The method of claim 93, further comprising removing exposed regions of said layer of insulative material through said layer of polysilicon.

98. The method of claim 97, wherein said removing said exposed regions of said layer of insulative material comprises etching said exposed regions of said layer of insulative material.

99. The method of claim 98, wherein said etching comprises dry etching said exposed regions of said layer of insulative material.

100. The method of claim 98, wherein said etching comprises anisotropically etching said exposed regions of said layer of insulative material.

101. The method of claim 71, further comprising doping at least one source region and at least one drain region of the semiconductor substrate, said at least one source region and said at least one drain region disposable adjacent the gate on opposite sides thereof.

102. The method of claim 17, wherein said removing comprises exposing said insulating structure around said terminal sites.

103. The method of claim 17, wherein said removing comprises exposing said insulating structure beneath said areas.

104. The method of claim 71, wherein said removing comprises exposing an insulating structure around said terminal sites.

105. The method of claim 71, wherein said removing comprises exposing an insulating structure beneath said areas.

RELATED PROCEEDINGS APPENDIX

Paper No. 43

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte KENNETH W. MARR

Appeal No. 2005-0026
Application No. 09/277,893

ON BRIEF

Before GARRIS, OWENS, and WALTZ, Administrative Patent Judges.
WALTZ, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal from the primary examiner's final rejection of claims 17 through 33, 50 through 72, and 74 through 101, which are all of the claims pending in this application. We have jurisdiction pursuant to 35 U.S.C. § 134.

According to appellant, the invention is directed to a method of fabricating a fuse where a layer of conductive material is deposited adjacent an insulative structure, the conductive material is patterned to define at least two discrete spaced

apart regions with the underlying insulative structure exposed between these spaced apart regions, and a layer of a metal silicide or polycide is formed over the conductive material and the exposed region (Brief, page 5). This layer of silicide or polycide is then patterned to define the upper layer of the terminals and the more narrow central region of the fuse (*id.*).[1]

Appellant states that the claims on appeal should be grouped into three groups (Brief, page 8). To the extent appellant presents specific, substantive arguments for the separate patentability of an individual claim or group of claims, we consider these claims separately. See 37 CFR § 1.192(c)(7)(2002); *In re McDaniel*, 293 F.3d 1379, 1383, 63 USPQ2d 1462, 1465 (Fed. Cir. 2002). Representative independent claim 17 is reproduced below:

17. A method of fabricating a fuse upon a semiconductor device, comprising:
disposing a layer of conductive material over an insulative structure of the semiconductor device;
patterning said layer of conductive material to define at least two laterally discrete, spaced apart

regions of conductive material between and around which said insulative structure is exposed;

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[1]The fuse per se has been claimed in a divisional application (S.N. 09/702,583)(Brief, page 2). This application was the subject of Appeal No. 2004-0033, with a decision mailed Jan. 2, 2004 (Paper No. 20), affirming all rejections on appeal.

disposing a layer of metal silicide over the semiconductor device, including adjacent to said at least two regions and to said insulative structure exposed between and around said at least two regions; and

patterning said layer of metal silicide so as to define at least two terminal regions of the fuse, each of which is in contact with a corresponding one of said at least two regions of conductive material, and a central region disposed between said at least two terminal regions and in contact with said insulative structure.

The examiner has relied on the following references as evidence of obviousness:

Fischer et al. (Fischer)	5,185,291	Feb. 09, 1993
Sandhu	5,231,056	Jul. 27, 1993
Degelormo et al. (Degelormo)	5,242,859	Sep. 07, 1993
Chen	5,712,206	Jan. 27, 1998
Ukeda et al. (Ukeda)	6,069,055	May 30, 2000
Mitani (published Japanese *Kokai* Patent Application)[2]	58-27569	Sep. 03, 1984

The following rejections are before this merits panel for review in this appeal:

(1) claims 17-33, 50-72 and 74-101 stand rejected under 35 U.S.C. § 112, ¶1, as containing subject matter which was not described in the original specification in such a way as to reasonably convey to one skilled in the art that the appellant had possession of the invention as now claimed at the time of filing (Answer, page 4);

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[2]We rely upon and cite from a full English translation of this document, previously made of record.

(2) claims 17, 19-24 and 26-33 stand rejected under 35 U.S.C. § 103(a) over Fischer in view of Chen (Answer, page 5);

(3) claim 18 stands rejected under § 103(a) over Fischer in view of Chen and Mitani (Answer, page 8);

(4) claim 25 stands rejected under § 103(a) over Fischer in view of Chen and Sandhu (*id.*);

(5) claims 50, 51, 55-60 and 62-68 stand rejected under § 103(a) over Fischer in view of Chen and Mitani (Answer, page 9);

(6) claims 52-54, 69 and 70 stand rejected under § 103(a) over Fischer in view of Mitani, Chen and Degelormo (Answer, page 12);

(7) claim 61 stands rejected under § 103(a) over Fischer in view of Mitani and Chen and Sandhu (Answer, page 13);

(8) claims 71, 74-86, 88-96 and 101 stand rejected under § 103(a) over Mitani in view of Fischer and Chen (*id.*);

(9) claim 72 stands rejected under § 103(a) over Mitani in view of Fischer, Chen and Degelormo (Answer, page 17);

(10) claim 87 stands rejected under § 103(a) over Mitani in view of Fischer, Chen and Sandhu (*id.*);

(11) claims 97-100 stand rejected under § 103(a) over Mitani in view of Fischer, Chen and Ukeda (Answer, page 18).

Based on the totality of the record, we *affirm* the examiner's rejection based on section 112, first paragraph, essentially for the reasons stated in the Answer and as set forth below. We *reverse* all of the rejections on appeal based on section 103(a) essentially for the reasons stated in the Brief, Reply Brief and those reasons set forth below. Accordingly, the

decision of the examiner to reject the claims on appeal is *affirmed.*

OPINION

A. The Rejection under § 112, ¶1

The examiner concisely and correctly states the issue as "whether or not there is support in the originally filed specification for [the claimed] 'laterally discrete spaced apart regions of said first layer of conductive material *around and between which* an underlying insulative structure is exposed' [emphasis added]." Answer, page 19. The examiner finds that there is no support in the specification that the insulative structure is exposed around and between the regions, nor has appellant pointed to any support for this claimed limitation (*id.*). More specifically, the examiner finds that Figure 4 only depicts layer 14 spaced apart from itself and appellant has not pointed to any original disclosure or suggestion that any portion of the insulating layer is exposed around spaced apart regions of the patterned conductive layer 14 (Answer, page 20).

Appellant argues that the spaced apart regions 14a and 14b are shown in the original drawings as being "laterally discrete"

from each other (Brief, page 11, citing Figures 6-8). Appellant further argues that the specification clearly provides that the polysilicon is disposed as discrete regions or portions that are substantially isolated from each other (Brief, page 11; Reply Brief, page 3, citing the specification at page 4, l. 27-page 5, l. 1).

An *ipsis verbis* disclosure is not necessary to satisfy the written description requirement of section 112, first paragraph. The disclosure need only reasonably convey to one of ordinary skill in the art that the inventor had possession of the subject matter in question at the time of filing. *See In re Edwards,* 568 F.2d 1349, 1351-52, 196 USPQ 465, 467 (CCPA 1978). The original drawings may provide "written description" of the claimed subject matter as required by section 112. *See Vas-Cath Inc. v. Mahurkar,* 935 F.2d 1555, 1565, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991); *Ex parte Holt,* 19 USPQ2d 1211, 1213 (Bd. Pat. App. & Int. 1991).

Appellants argue that the original specification teaches that "the polysilicon that underlies the terminal regions of the fuse is disposed on the insulative structure in discrete regions or portions that are substantially <u>isolated</u> from one another" (page 4, l. 27-page 5, l. 1, underlining added)(Brief, page 11;

Reply Brief, page 3)[3]. As also taught in the original specification, "the underlying insulative structure is exposed between the at least two spaced apart regions of the layer of conductive material" (page 5, ll. 12-14, underlining added; see also page 7, ll. 12-15).

As correctly found by the examiner, appellant's Figure 4 depicts patterning of the first conductive layer (polysilicon) while Figure 6 relates to a further step of patterning the metal silicide to form the fuse and gate structures (Answer, page 20; see the specification, page 9, l. 16-page 10, l. 14 and page 11, l. 7-page 12, l. 3). The examiner correctly argues that Figure 4 shows layer 14 as a continuous layer, with no insulative structure around it (Answer, pages 20-21). The examiner is also correct that appellant has not labeled the "laterally discrete spaced apart regions" as 14a and 14b in Figure 4, as appellant did for Figures 7 and 8 (Answer, page 20).

We determine that the examiner has established that Figure 4, and its corresponding disclosure in the specification, depicts

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[3]We also note that appellant presents arguments concerning the objections to the drawings and the specification (Brief, pages 9-11). As correctly noted by the examiner (Answer, page 3, ¶(6)), these issues are petitionable, not appealable. *See MPEP*, § 1002.02(c) and § 1201, 8th ed., Rev. 2, May 2004.

patterning a layer of conductive material to define at least two lateral spaced apart regions *between* which the insulative structure is exposed. Accordingly, the examiner has met the initial burden of establishing why persons skilled in the art would not recognize in the disclosure a description of the invention as now claimed. *See In re Alton,* 76 F.3d 1168, 1175, 37 USPQ2d 1578, 1583 (Fed. Cir. 1996). Therefore the burden of coming forth with evidence or arguments shifts to appellant. *See In re Alton, supra.* As correctly noted by the examiner (Answer, page 20), appellant's argument that Figures 6-8 describe the spaced apart regions 14a and 14b is not well taken (Brief, page 11). Figures 6-8 are directed to patterning of the metal silicide and forming the fuse and gate structures (see the specification, page 11, l. 7-page 13, l. 10). The language in question relates to "patterning said layer of conductive material" that is over an insulative structure to form the spaced apart regions between which the insulative structure is exposed (see claim 17 on appeal). As correctly found by the examiner (Answer, page 20), this patterning step is depicted by Figure 4, which fails to show that the lateral spaced apart regions are "discrete" or that the insulative structure is exposed "around"

the regions (see also the specification, page 9, l. 16-page 10, l. 14).

Appellant also argues that the examiner inappropriately limits the relevant description to the Figures and does not consider the "as-filed specification" as a whole (Reply Brief, page 2). This argument is also not well taken. As discussed above, the accompanying disclosure in the specification has been considered along with the depictions of the invention in the Figures. Contrary to the argument in the Reply Brief mentioned above, appellant admits that the accompanying disclosure "does not itself explain that these regions are laterally discrete from one another" (Brief, page 11). Furthermore, as discussed above, the original disclosure does not explain that the insulative structure is exposed between *and* around these regions during the patterning step (the only description refers to exposure of the insulative structure "between" these regions during the patterning step; see the specification, page 5, ll. 12-14).

Appellant argues that the disclosure that the regions are discrete and "substantially isolated" from one another would provide basis or support for the subject matter in question (Reply Brief, page 3). Appellant also argues that it would be "inherent" that when the first layer of conductive material is

patterned to form laterally discrete spaced apart regions, the underlying insulative structure would be exposed around and between these regions (Reply Brief, page 4). These arguments are not persuasive. Appellant has not established that the disclosed term "substantially isolated" refers to the regions as they are first patterned rather than the final structure or steps as shown in Figures 6-8. Additionally, this term "substantially isolated" has not been defined in the specification as meaning that the insulative structure is exposed "between and around" these regions. Appellant's argument that the exposure of the insulative structure around and between the regions would be "inherent" is not persuasive since it has not been established that the lateral spaced apart regions of Figure 4 are "discrete."

For the foregoing reasons and those stated in the Answer, we determine that the examiner has met the initial burden of establishing a failure to fulfill the "written description" requirement of section 112, first paragraph. Based on the totality of the record, including due consideration of appellant's arguments, we determine that the originally filed specification and figures do not convey with reasonable clarity to those of ordinary skill in the art at the time of filing that appellant was in possession of the invention as now claimed.

Therefore we affirm the examiner's rejection of all the claims on appeal under 35 U.S.C. § 112, first paragraph, for failure to fulfill the "written description" requirement.

B. The Rejections under § 103(a)

With regard to the rejection of claim 17, the examiner finds that Fischer discloses disposing a layer of conductive material over an insulative structure of a semiconductor device, patterning the layer of conductive material to define at least two spaced apart regions of conductive material through which the insulative structure is exposed, disposing a second conductive layer over the patterned layers, and patterning the second conductive layer so as to define at least two terminal regions of the fuse and a central region disposed between the terminal regions (Answer, pages 5-6). The examiner recognizes that Fischer discloses that the second conductive layer may be a metal such as aluminum or tungsten, or may be polysilicon (Answer, page 23, citing col. 2, ll. 43-45 and 59-63). The examiner applies Chen as evidence that alternate materials may be used as the fuse, specifically teaching the use of polysilicon, aluminum, metal silicides, and polycides, with a preference for tungsten silicide (Answer, pages 6 and 23, citing Chen col. 5, ll. 59-63). From these findings, the examiner concludes that it would have

been obvious to one of ordinary skill in this art at the time of appellant's invention to use the metal silicide fuse material taught by Chen for the fuse material in the method of forming a fuse as disclosed by Fischer (Answer, pages 6 and 23-24).

Appellant argues that the patterning of the first conductive layer of Fischer does not result in the formation of "laterally discrete spaced apart regions" such as appellant's regions 14a and 14b (Brief, page 14).

Appellant also argues that both Fischer and Chen lack any teaching or suggestion of patterning a conductive layer to define at least two "laterally distinct, spaced apart regions between and around which an underlying insulative structure is exposed" (Brief, sentence bridging pages 17-18). We agree.

The examiner finds that the insulative structure of Fischer is exposed "*between* the at least two regions" (Answer, page 5, italics added). The examiner has not cited any reference which discloses or suggests patterning a conductive layer to define at least two "laterally discrete, spaced apart regions between and around which an underlying insulative structure is exposed" (see the Answer in its entirety). Rather, the examiner has stated:

> It has been shown that at least "around and between which an underlying insulative structure is exposed" is not supported in the originally filed specification. Clearly this aspect of the limitation can not be understood as it relates to the presently claimed invention. Therefore, this aspect of the limitation has not been addressed in the rejection. [Answer, page 27].

This position by the examiner ignores a limitation of the claims.[4] In determining the patentability of a claim against the prior art, all of its limitations, whether supported by the original disclosure or not, must be considered. *See Ex parte Grasselli,* 231 USPQ 393, 394 (Bd. App. 1983); *cf., In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

For the foregoing reason, we determine that the examiner has not established a *prima facie* case of obviousness. Thus we cannot sustain the rejection over Fischer in view of Chen. We also cannot sustain the rejections involving the secondary references to Mitani, Sandhu, Degelormo, and Ukeda since these references do not remedy the deficiency noted above with regard to Fischer and Chen. Similarly, the rejections employing Mitani as a primary reference do not consider the limitation of the

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[4]Every independent claim on appeal contains the disputed language discussed in the section 112 rejection above.

independent claims as discussed above. Therefore we reverse all of the rejections on appeal based on 35 U.S.C. § 103(a).

C. Summary

The rejection of claims 17-33, 50-72 and 74-101 under 35 U.S.C. § 112, ¶1, is affirmed.

The following rejections under 35 U.S.C. § 103(a) have been reversed:

(1) claims 17, 19-24 and 26-33 over Fischer in view of Chen;

(2) claim 18 over Fischer in view of Chen and Mitani;

(3) claim 25 over Fischer in view of Chen and Sandhu;

(4) claims 50, 51, 55-60 and 62-68 over Fischer in view of Chen and Mitani;

(5) claims 52-54, 69 and 70 over Fischer in view of Mitani, Chen and Degelormo;

(6) claim 61 over Fischer in view of Mitani, Chen and Sandhu;

(7) claims 71, 74-86, 88-96 and 101 over Mitani in view of Fischer and Chen;

(8) claim 72 over Mitani in view of Fischer, Chen and Degelormo;

(9) claim 87 over Mitani in view of Fischer, Chen and Sandhu; and

(10) claims 97-100 over Mitani in view of Fischer, Chen and Ukeda.

The decision of the examiner is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv)(effective Sep. 13, 2004; 69 Fed. Reg. 49960 (Aug. 12, 2004); 1286 Off. Gaz. Pat. Office 21 (Sep. 7, 2004)).

AFFIRMED

BRADLEY R. GARRIS
Administrative Patent Judge)

TERRY J. OWENS
Administrative Patent Judge) BOARD OF PATENT APPEALS AND INTERFERENCES

THOMAS A. WALTZ
Administrative Patent Judge)

TAW/jrg

Appeal No. 2005-0026
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Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KENNETH W. MARR

Appeal No. 2004-0033
Application No. 09/702,583

ON BRIEF

Before GARRIS, OWENS, and WALTZ, Administrative Patent Judges.
WALTZ, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal from the primary examiner's refusal to allow claims 1 and 3 through 32 as amended subsequent to the final rejection (see the amendment dated Nov. 4, 2002, Paper No. 12, entered as per the Advisory Action dated Nov. 19, 2002, Paper No. 13). Claims 1 and 3-32 are the only claims remaining in this application. We have jurisdiction pursuant to 35 U.S.C. § 134.

According to appellant, the invention is directed to fuses and semiconductor devices that include such fuses, where each fuse includes a central, or fusible, region positioned between two

terminal regions, with the central region including a single layer of a metal silicide or polycide (Brief, page 4).

As correctly noted by the examiner (Answer, page 3), appellant's statement in the Brief (page 6) regarding the grouping of the claims is contradictory. Since appellant has not stated reasonably specific, substantive reasons for the separate patentability of any individual claim (see the Brief and Reply Brief in their entirety), we select one claim from each ground of rejection and decide the grounds of rejection on the basis of these claims alone. See 37 CFR § 1.192(c)(7)(2000); *In re McDaniel*, 293 F.3d 1379, 1383, 63 USPQ2d 1462, 1465 (Fed. Cir. 2002). Illustrative independent claim 1 is reproduced below:

1. A fuse of a semiconductor device, comprising:
a central region comprising metal silicide and contacting an insulative structure of the

semiconductor device, said central region being configured to become discontinuous

upon application of at least a programming electrical current thereacross; and

two terminal regions, a first of said two terminal regions being disposed adjacent a first end of

said central region and a second of said two terminal regions being disposed adjacent a

second end of said central region, each of said two terminal regions being separated from

said insulative structure by a layer of conductive material.

The examiner has relied upon the following references as evidence of obviousness:

Lim	4,491,860	Jan. 01, 1985
Fischer et al. (Fischer)	5,185,291	Feb. 09, 1993
Ogawa	5,585,662	Dec. 17, 1996
Chen	5,712,206	Jan. 27, 1998

Claims 1, 3, 5-13, 15-22 and 25-27 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Fischer in view of Chen (Answer, page 4). Claims 4, 14, 23 and 24 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Fischer in view of Chen and Lim (Answer, page 7). Claims 28-32 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Fischer in view of Chen and Ogawa (*id.*). We *affirm* all of the examiner's rejections on appeal essentially for the reasons stated in the Answer and those reasons set forth below.

OPINION

A. The Rejection over Fischer and Chen

The examiner finds that Fischer discloses a fuse of a semiconductor device comprising a central region made of polysilicon, aluminum or tungsten, where the central region contacts an insulative structure 10 and becomes discontinuous upon application of at least a programming electrical current (Answer,

page 4). The examiner further finds that Fischer discloses first and second terminal regions disposed adjacent a first and second end of the central region, respectively, where each of the two terminal regions are separated from the insulative structure 10 by a layer of conductive material 11 (*id.*).

The examiner recognizes that Fischer does not disclose or teach that the central region of the fuse is made of a metal silicide as required by claim 1 on appeal (Answer, sentence bridging pages 4-5). The examiner finds that Chen teaches that metal silicides are an alternate material for use as a fuse central region in place of aluminum or polysilicon (Answer, page 5). From these findings, the examiner concludes that it would have been obvious to one of ordinary skill in this art to use metal silicides, as taught by Chen, in place of the aluminum or polysilicon central region of the fuse disclosed by Fischer (*id.*). We agree.

Appellant argues that one of ordinary skill in the art would not have been motivated to combine the teachings of Fischer and Chen in the manner proposed by the examiner, and that the asserted motivations are "extremely broad." Brief, page 9 (see also the Reply Brief, page 4). These arguments are not well taken since the examiner specifically states that the motivation to replace the

central region of the fuse of Fischer with the central region material of Chen is that the art has recognized that these central region materials are "alternate materials" or equivalent materials (Answer, pages 5 and 9-10). It is well settled that an express suggestion to substitute one equivalent for another need not be present to render such a substitution obvious. *See In re Fout*, 675 F.2d 297, 301, 213 USPQ 532, 536 (CCPA 1982). Furthermore, as noted by the examiner (Answer, pages 9-10), both Fischer and Chen teach the use of polysilicon and aluminum as central region material for a fuse, with Chen additionally teaching the use of metal silicides.

Appellant argues that Fischer and Chen are directed to different fuse structures, with Fischer teaching a fuse with terminal regions that include two layers while Chen teaches a fuse with terminal regions that merely include a single layer (Brief, page 10). Appellant thus submits that there would be no reason for one of ordinary skill in the art to substitute the fuse of Chen for the fuse of Fischer (*id.*).

This argument is not persuasive for reasons set forth by the examiner on pages 9 and 12-13 of the Answer. The test for obviousness is not whether the entire structure of the secondary reference may be bodily incorporated into the structure of the

primary reference but what the combined teachings of the prior art would have suggested to one of ordinary skill in the relevant art. *See In re Keller,* 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). As found by the examiner and apparently not contested by appellant, Fischer discloses every limitation of claim 1 on appeal except that the central region comprises a metal silicide (Answer, page 9; Reply Brief, page 3). Chen was relied upon for its teaching that other materials such as metal silicides are equivalent to polysilicon and aluminum for use as the central region of a fuse, capable of being "blown" by electrical current or laser pulses (Answer, page 12). The test for obviousness does not require that the structure of Chen is the same as the structure of Fischer. *See In re Keller, supra.*

Appellant argues that the teachings of Fischer are directed to a fuse which is clearly configured to be "blown" by applying a programming current thereto, while the fuse taught in Chen has a configuration which is more amenable to being "blown" with a laser (Brief, pages 10 and 12). As correctly noted by the examiner (Answer, page 13), this argument is not well taken since both Fischer and Chen teach that their fuses can be "blown" by either electrical current or a laser pulse (see Fischer, abstract; col. 4, ll. 9-14; Chen, col. 4, ll. 53-54).

For the foregoing reasons and those reasons set forth in the Answer, we determine that the examiner has established a *prima facie* case of obviousness in view of the reference evidence. Based on the totality of the record, including due consideration of appellant's arguments, we determine that the preponderance of evidence weighs most heavily in favor of obviousness within the meaning of section 103(a). Accordingly, we affirm the examiner's rejection of claim 1, and claims 3, 5-13, 15-22, and 25-27 which stand or fall with claim 1, under 35 U.S.C. § 103(a) over Fischer in view of Chen.

B. The Rejections over Fischer, Chen, Lim and Ogawa

With respect to the rejection of claims 4, 14, 23 and 24 under section 103(a) over Fischer, Chen and Lim, as well as the rejection of claims 28-32 under section 103(a) over Fischer, Chen and Ogawa, appellant does not specifically argue any individual claim or present any new arguments, merely relying on the arguments discussed above (Brief, page 13). Accordingly, we adopt our comments from above, as well as the findings and reasoning from the Answer, and affirm each of these rejections.

C. Summary

The rejection of claims 1, 3, 5-13, 15-22 and 25-27 under 35 U.S.C. § 103(a) over Fischer in view of Chen is affirmed. The rejection of claims 4, 14, 23 and 24 under 35 U.S.C. § 103(a) over Fischer in view of Chen and Lim is affirmed. The rejection of claims 28-32 under 35 U.S.C. § 103(a) over Fischer in view of Chen and Ogawa is affirmed.

The decision of the examiner is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

BRADLEY R. GARRIS)
Administrative Patent Judge)
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) BOARD OF PATENT
TERRY J. OWENS) APPEALS
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) INTERFERENCES
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THOMAS A. WALTZ)
Administrative Patent Judge)

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